SPECIFICATION AMENDMENTS

Please newly add the following paragraph following the title of the specification as originally filed.

CROSS-REFERENCE TO RELATED APPLICATIONS

This invention is a continuation of U.S. Patent Application Serial No. 09/467,207, entitled "Dual Damascene Interconnect Structure Using Low Stress Fluorosilicate Insulator With Copper Conductors," now abandoned, which is a continuation-in-part of U.S. Patent Application Serial No. 08/744,846, entitled "Fluorine-Free Barrier Layer Between Conductor and Insulator for Degradation Prevention," now U.S. Patent No. 6,310,300, both of which are assigned to the same assignee. The specification of U.S. Patent Application Serial No. 09/467,207 and U.S. Patent No. 6,310,300 are each incorporated herein in its entirety.

Please replace the paragraph that begins on page 8, line 18 and ends on page 9, line 18 with the following replacement paragraph:

Referring to the figures generally and figure 1 specifically, there is shown a representation of a typical line/via structure. The line portion, 1, has a height represented by h_l, and the via portion, 5, has a height represented by h_v . The overall height of the structure, h_t equals $h_v + h_l$. When forming the structure of the instant invention, as shown in figure 2, a layer of a first undoped insulator, 10, is deposited according to any means known in the art. The height of the undoped layer should not be equal to h_t. A substantial portion of the beneficial effects of the structure as outlined in this invention are not achieved when the height of the undoped layer is sign greater than height of the via, h_v. It is preferable if the height of the undoped material is significantly less than the height of the via, h_v,. A second insulating layer of a doped insulating material, 15, is then deposited. The height of the doped layer should be equal to $h_t - h_v$. One of the objectives of the instant invention is to balance mechanical stress needs with increased interconnect capacitance. The balance of those two should be kept in mind when choosing the thicknesses of the doped and undoped materials. Also in a preferred embodiment, a layer of capping layer, 20, would be deposited prior to the deposition of the undoped first

insulating layer. The maximum via height, h_v should then be greater than - the height of the undoped insulating material plus the capping layer material.

Please replace the paragraph that begins on page 9, line 19 and ends on page 10, line 23 with the following replacement paragraph.

The undoped insulating material can be selected from any material known in the art. Preferably, the undoped insulating material would be any silicon dioxide based film which is compatible with back end of the line (BEOL) processing and does not contain any significant fluorine content, whether intentional or unintentional. More preferably, the undoped insulating material would be undoped silica glass (USG). Most preferably, the undoped material would be plasma enhanced chemical vapor deposited (PECVD) silica glass from silane or tetraethylorthosilicate (TEOS) precursors. The doped insulating material can be selected from any material where the use of the material causes capacitance/stress tradeoffs. In a preferred embodiment, the final structure should have a mean compressive stress (as- deposited) of between $O.8E^9$ and $1.4E^9$ dynes/cm^2. Preferably, the doping would be fluorine. The fluorinated insulators could be any insulator with sufficient fluorine content to have a risk of degradation when integrated with metallization susceptible to fluorine poisoning. The fluorinated insulating material could be any of the following, including but not limited to, fluorinated silicon dioxide, fluorinated amorphous or diamondlike carbon or fluorinated organic polymers. Preferably, the doped insulating material would be fluorinated silica glass (FSG). The capping material could be any material with suitable etch selectivity relative to the chosen undoped insulator, appropriate copper diffusion barrier properties and other properties compatible with BEOL processes. An example of preferred embodiment capping layer materials include, but are not limited to silicon nitride, silicon carbide or hydrogenated silicon carbide. Preferably, the capping layer would comprise silicon nitride Si_xN_y.

Please replace the paragraph that begins on page 11, line 14 and ends on page 12, line 5 with the following replacement paragraph:

In the instant invention(we are presupposing that $h_v = 0.6\mu m$)

and h_t = 0.4 µm. An underlying wire 40, in an underlying wiring level, 45 is capped with 700A of silicon nitride[,]. A 0.4µ[u]m layer of undoped silica glass (USG) is then deposited. A layer of doped silica glass, FSG, O.53µm, is then deposited. The FSG film which is used is a dual frequency PECVD film, deposited from SiH_4, N_20 inert carrier gases and SIF_4 as the fluorine doping gas. The deposition is at 380-400C, with 2000W of total RF power. The dielectric constant of the film is about 3.75, the refractive index is about 1.445 and the as deposited stress of the film is about $1.5E^9$ /dynes/cm_2 in the compressive direction. The USG film is a single frequency PECVD film, deposited from SiH_4, N_2O and inert carrier gases. The deposition is at 380-400C, with 1100W of total power. The dielectric constant is about 4.1, the refractive index is about 1.46 and the stress is about $0.8E^9$ in the compressive direction.